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Hybrid Nanodielectrics for Low-Voltage Organic Electronics

*Alessandro Luzio, Francisco García Ferré, Fabio Di Fonzo, and Mario Caironi**

Nanoscale hybrid dielectrics composed of an ultra-thin polymeric low-κ bottom layer and an ultra-thin high-κ oxide top layer, with high dielectric strength and capacitances up to 0.25 μFcm^{-2}, compatible with low-voltage, low-power, organic electronic circuits are demonstrated. An efficient and reliable fabrication process, with 100% yield achieved on lab-scale arrays, is demonstrated by means of pulsed laser deposition (PLD) for the fast growth of the oxide layer. With this strategy, high capacitance top gate (TG), n-type and p-type organic field effect transistors (OFETs) with high mobility, low leakage currents, and low subthreshold slopes are realized and employed in complementary-like inverters, exhibiting ideal switching for supply voltages as low as 2 V. Importantly, the hybrid double-layer allows for a neat decoupling between the need for a high capacitance, guaranteed by the nanoscale thickness of the double layer, and for an optimized semiconductor–dielectric interface, a crucial point in enabling high mobility OFETs, thanks to the low-κ polymeric dielectric layer in direct contact with the polymer semiconductor. It is shown that such decoupling can be achieved already with a polymer dielectric as thin as 10 nm when the top oxide is deposited by PLD. This paves the way for a very versatile implementation of the proposed approach for the scaling of the operating voltages of TG OFETs with very low level of dielectric leakage currents to the fabrication of low-voltage organic electronics with drastically reduced power consumption.

1. Introduction

Organic field-effect transistors (OFETs) give access to electronic applications, such as logic circuits, backplanes, sensors and light-emitting devices,[1–4] with peculiar and appealing properties like lightness, flexibility and (semi)transparency.[5] Moreover low-temperature processing drastically reduces costs and the environmental impact of manufacturing. For all these reasons OFETs have been extensively studied and developed with the aim to realize innovative electronic products where low-cost, lightness, flexibility and ease of integration are driving factors (e.g. radio-frequency identification tags, wearable, portable and/or disposable electronics etc.). High voltage (50–100 V) polymer-based OFETs with carrier mobilities equal to or even superior to 1 cm^{2}V^{-1}s^{-1} have been widely demonstrated;[6–13] however, proper downscaling strategies are required to transfer such good performances to OFETs capable of operating at just 1 V or 2 V, which are voltage levels required for several applications of practical interest[14] and for the fabrication of organic electronics with drastically reduced power consumption, a condition of utmost importance for portable devices.[15–17]

A great number of the existing strategies for low voltage OFETs are restricted to bottom-gate (BG) configurations,[15,18–21] where the semiconductor is deposited on top of a pre-processed dielectric. This is due to the fact that most commonly applied high capacitance dielectrics (high-κ physically deposited or sintered oxides and/or self assembled monolayers) hardly match top-gate (TG) processing requirements, where the dielectric has to be processed on top of the thin organic semiconductor film instead. However, a diversification of the device architecture is indeed desirable, because on the one side optimized charge injection[22–24] and transport[13] properties can be attained, and on the other more solutions to processing and patterning issues in complex circuitry are available. Therefore, a major breakthrough in the fabrication of TG low-voltage OFETs would strongly contribute to easily transfer the optimized performances observed in high voltage organic transistors to devices of practical use.

A numbers of solutions have been proposed in this direction, comprising a limited number of high-κ polymeric dielectrics, mostly within the ferroelectric polyvinylidene difluoride family.[25,26] However, high-κ dielectrics were shown to degrade the transport properties of many organic semiconductors, likely due to the induced dipoles disorder causing a broadening of the density of states (DOS) at the semiconductor/dielectric interface.[25,27–31] The presence of side chains in highly ordered polymeric semiconductors apparently represents a *synthetic* way to preserve the interface from the broadening of the DOS;[25,32] however, a more general approach would reduce the constraints on the π-conjugated materials synthesis. Alternatively, the use of solution processed electrolytes (polyelectrolites,[33–37] iongels)[38–42] to gate OFETs represents a very promising approach for attaining ultra-low voltage operation. In this case there are open questions about the long-term stability of devices, which

Dr. A. Luzio, F. García. Ferré,
Dr. F. Di Fonzo, Dr. M. Caironi
Center for Nano Science and Technology @PoliMi
Istituto Italiano di Tecnologia
Via Pascoli 70/3, 20133, Milano, Italy
E-mail: mario.caironi@iit.it
F. G. Ferré
Dipartimento di Energia
Politecnico di Milano
Via Ponzio 34/3, 20133, Milano, Italy

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might undergo electrochemical doping,[43,44] and their frequency operation, since the gating response time is intrinsically dependent on the movement of ions in the electrolyte.[40]

In this work we illustrate a simple, high yield, low-temperature method to fabricate hybrid nanoscale dielectrics compatible with ultra-low voltage operation of high mobility TG OFETs. This method consists on the fabrication of a double-layered hybrid dielectric composed as follows: an ultra-thin (~10 nm) organic dielectric coupled with an ultra-thin (~30 nm) high-κ oxide as the top layer. The bilayer strategy allows for an effective decoupling of the physicochemical characteristics of the semiconductor/dielectric interface from critical parameters for low voltage operation, like the capacitance and the dielectric strength.[45] More in details, the organic low-κ layer, like poly(methyl methacrylate) (PMMA, $\kappa = 3.6$) or polystyrene (PS, $\kappa = 2.6$), in direct contact with the active phase guarantees a narrow DOS at the interface; the top high-κ oxide layer ensures at the same time a suitably high break-down voltage and a high capacitance to the hybrid dielectric stack, thus enabling a reliable low voltage operation. While a similar double layer strategy has been recently demonstrated in the case of graphene-based OFETs[46] and BG devices,[47–51] no effective ultra-thin dielectric bilayer was demonstrated for low voltage TG polymeric OFETs so far, a critical aspect being represented by the oxide deposition technique which must be compatible with the underlying organic materials. Kippelen *et al*. employed Atomic Layer Deposition (ALD) to deposit alumina on the top of a Cytop layer in TG OFETs with a maximum capacitance of ~35 nFcm^{-2} (total dielectric thickness ~90 nm), which hindered operation below 10 V – 15 V.[52,53]

In this work, we adopted pulsed lased deposition (PLD) to deposit the high-κ oxide layer, here alumina. PLD is a versatile, plasma-based deposition process that can be carried out at room-temperature. The process is compatible with organic substrates[54] and is particularly suited for producing complex oxides with a stoichiometric transfer from the target to the substrates.[55–57] It is worth highlighting that typical deposition rates for Al_2O_3 by PLD are around 0.85 nm s^{-1},[58] higher than typical rates for ALD (0.1 nm s^{-1}).[59] Furthermore, even higher deposition rates could be obtained by increasing pulse frequency.

High yield and high control over the fabrication process were attained for both *p*-channel poly(2,5-bis(3-alkylthiophen-2-yl) thieno[3,2-b]thiophene (pBTTT)[32,60–62] and *n*-channel poly{[*N*,*N*′-bis(2-octyl-dodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} (P(NDI2OD-T2))[13,63] low-voltage OFETs with capacitances up to 0.25 μFcm^{-2}. P(NDI2OD-T2) is a very well-known high mobility *n*-type polymeric semiconductor whose performances can be strongly affected by processing conditions[64] and by the presence of dipoles at the interface with the dielectric layer. Thanks to the hybrid nanodielectrics here developed, P(NDI2OD-T2) OFETs that are completely switched ON already at 1 V with unprecedented intrinsic linear mobility of ~0.7 cm^{2}V^{-2}s^{-1} were obtained. This demonstrates that the energetics at the semiconductor-dielectric interface are entirely dominated by the ultra-thin, bottom organic interlayer of the dielectric stack, thus making the proposed technique very versatile. Finally, we demonstrate the possibility to use this technique to realize complementary inverters exhibiting an inverting gain (defined as the absolute value of the derivative of the inverter output voltage with respect to the input voltage) higher than 10 for supply voltages as low as 2 V.

2. Results and Discussion

As a preliminary study, we performed an electrical characterization of parallel plate capacitors based on PLD-grown Al_2O_3, which was sandwiched between two electrodes. We consistently extracted a relative permittivity $\kappa = 8.5$ from 600 nm and 30 nm thick alumina films on different flexible (polyethylene naphthalate, PEN) or rigid (Glass, SiO_2) substrates, which is consistent with previously reported values for Al_2O_3 grown by PLD in similar conditions.[65,66] An electrical breakdown field higher than 1 MV/cm was measured, a value which safely allows low voltage operation.

Hybrid dielectric bilayers were then fabricated, where the bottom layer is a solution processed PMMA layer (spin coating from 1-butyl acetate solution), on top of which a thin film of Al_2O_3 is deposited by means of PLD (**Figure 1**a). In Figure 1b

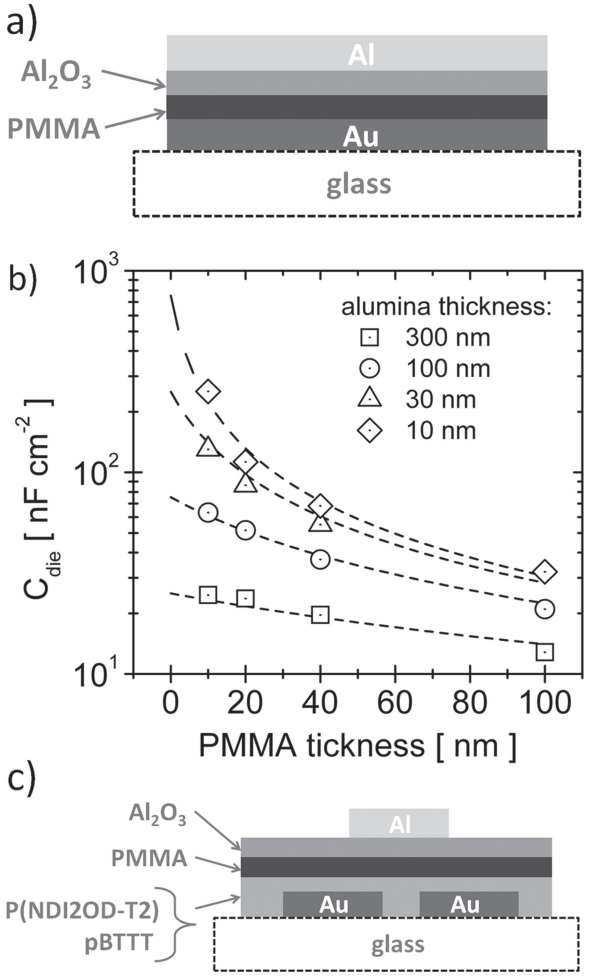

Figure 1. a) Sketch of the double-layered capacitors (PMMA + Al_2O_3 as dielectrics) that were fabricated and characterized in this work; b) capacitance vs. PMMA thickness of the capacitors at different values of alumina thickness; the theoretical capacitances of the series of the two layers is also reported (dashed lines); c) sketch of the staggered TG OFETs realized employing the double layer gate dielectrics.

the capacitance C_{die} of alumina/PMMA bilayer at different values of PMMA and alumina thicknesses is reported. A very good fitting of the measured data with the model of two capacitors in series was observed, being verified the following expression:

$$C_{die} = \left(C_{Al_2O_3}^{-1} + C_{PMMA}^{-1}\right)^{-1} \quad (1)$$

with C_{die} the measured capacitance per area of the bilayer, $C_{Al_2O_3}$ and C_{PMMA} the theoretical capacitance per area of alumina and PMMA layers respectively, calculated as:

$$C_{Al_2O_3} = \frac{\varepsilon_0 \kappa_{Al_2O_3}}{t_{Al_2O_3}} \quad (2)$$

$$C_{PMMA} = \frac{\varepsilon_0 \kappa_{PMMA}}{t_{PMMA}} \quad (3)$$

with ε_0 the vacuum permittivity, $\kappa_{Al_2O_3}$ the alumina relative permittivity, κ_{PMMA} the PMMA relative permittivity, $t_{Al_2O_3}$ the alumina layer thickness and t_{PMMA} the PMMA layer thickness. As reported in Figure 1b, this behavior was observed in the whole range of explored thicknesses (from 10 nm to 300 nm for the alumina, from 10 nm to 100 nm for the PMMA). The good matching of the hybrid dielectrics capacitance with the series capacitors model, down to thicknesses of only 10 nm for the PMMA layer, is a strong indication of the negligible penetration depth of alumina into the PMMA layer during PLD deposition. Such an ideal behavior emphasizes the integrity of the two layers composing the capacitors, which maintain their independent dielectric characteristics (dielectric constant) even after the deposition of the oxide.

We then studied the applicability of dielectrics comprising a PLD-grown layer in top-gate/bottom-contacts (TGBC) OFETs. Solution processed P(NDI2OD-T2) and pBTTT, two well known and studied model semiconducting polymers with relatively high carriers mobility, were employed to realize *n*-channel and *p*-channel OFETs respectively. First, a single layer of alumina was directly deposited onto the semiconductor surface. Despite the relatively "gentle" nature of PLD deposition and its compatibility with polymer insulating layers, as observed in bilayer capacitors, we have consistently measured very low field-effect mobility μ in these devices: orders of magnitude lower than in the case of optimized OFETs based on the same semiconductors. This result suggests that the direct deposition of alumina by PLD is strongly detrimental for charge transport in the conjugated polymer: indeed the top semiconductor surface is the most crucial area of the device because it is at this interface that the charges accumulate forming the channel which extends only a few molecular layers in depth. While we have not investigated in detail the process leading to degraded mobility, we can exclude that this is only an effect of a dipolar disorder induced by a high-κ dielectric, since especially pBTTT is known not be so strongly affected by this effect.[32] Therefore the degraded mobility might be the effect of even a very limited contamination of the channel region, as an inherent consequence of the PLD process. This therefore indicates the need for a protective interlayer (buffer) to avoid this negative effect on the transistors performances. The detailed description of these experiments is reported in the Supporting Information.

The above described hybrid dielectric layers (Figure 1a) were integrated in the same OFETs (Figure 1c) in order to take advantage of the compatibility of PMMA with optimized organic devices and of a neat separation between the two dielectrics forming the stack.

We have successfully tested OFETs integrating hybrid dielectrics with a broad range of capacitances, up to 0.25 μFcm^{-2}, by varying the thickness of both layers. A minimum PMMA thickness of 10 nm together with a minimum alumina thickness of 30 nm guarantees a highly reproducible fabrication with an outstanding yield for a lab-scale process: 100% working devices over 64 OFETs fabricated with channel lengths varying from 5 μm to 20 μm. Moreover, in all the cases dielectric breakdown occurred at V_g values much higher (at least 4×) than the minimum operative voltage of each device. Importantly, leakage currents through the dielectric layer lay at least three orders of magnitude below channel currents (a maximum leakage of ~10^{-7} A cm^{-2} was measured in OFETs with capacitance value of 0.25 μFcm^{-2} at V_g = 2 V), even if gate contacts were only coarsely patterned and the semiconductor layer was not patterned at all, details which strongly influence leakage currents.[67]

On top of this excellent dielectric performances, low voltage P(NDI2OD-T2) FETs showed ideal *n*-channel characteristics. In **Figure 2** the complete electrical characterization of P(NDI2OD-T2) device with a capacitance of ~80 nFcm^{-2}, obtained with a PMMA layer thickness of ~20 nm and an alumina thickness of 30 nm, is reported. We obtained an I_{ON}/I_{OFF} current ratio approaching 10^5 (calculated at V_g = 2 V for I_{ON} and at V_g = –1 V for I_{OFF}, keeping V_d = 2 V), and very modest maximum gate leakage currents (in Figure 2a inferior to 10^{-8}A cm^{-2} up to V_g = 2 V). Device are completely ON, i.e. displaying their maximum mobility, already at gate voltages 1.5 V beyond the onset (V_{on}), defined as the gate voltage for which the drain current starts to increase (in Figure 2a V_{on} = –1.2 V). An average apparent linear mobility μ of ~0.2 cm^{2}V^{-1}s^{-1} with a standard deviation of ~0.01 V, which is the OFET mobility disregarding contact resistances effect, was measured at V_g = 2 V. This is a state-of-the-art value for high voltage staggered TGBC P(NDI2OD-T2)-based OFETs and unprecedented in the case of low voltage operation[25] (Figure 2b). A mean threshold voltage (V_{th}) of –0.7 V (deviation standard ~ 0.2 V) was calculated in the linear regime, indicative of the bias needed to switch on the device. The output curves (Figure 2d) reveal good injection (no S-shape) and clear *n*-type current modulation. The subthreshold behavior of these devices is also noteworthy (Figure 2c): a subthreshold slope (*SS*) as low as ~100 mVdec^{-1} is displayed for capacitances as high as 130 nFcm^{-2}, a remarkable value compared to low-voltage OFETs in the literature.[15,48,68,69]

We employed scanning electron microscopy (SEM) to investigate in detail the stack of layers composing ultra-low voltage P(NDI2OD-T2) OFETs. **Figure 3**a shows the cross section of a device with a capacitance of 130 nFcm^{-2}. This is the highest capacitance value we obtained with a hybrid dielectric enabling a process yield of 100%. The SEM images confirm a 30 nm thick alumina layer, on top of the two organic layers of PMMA and P(NDI2OD-T2) which cannot be distinguished and that have an overall thickness of 40 nm. We have also performed an AFM characterization to check the homogeneity and the quality of the surface of each film. Figure 3b–d show

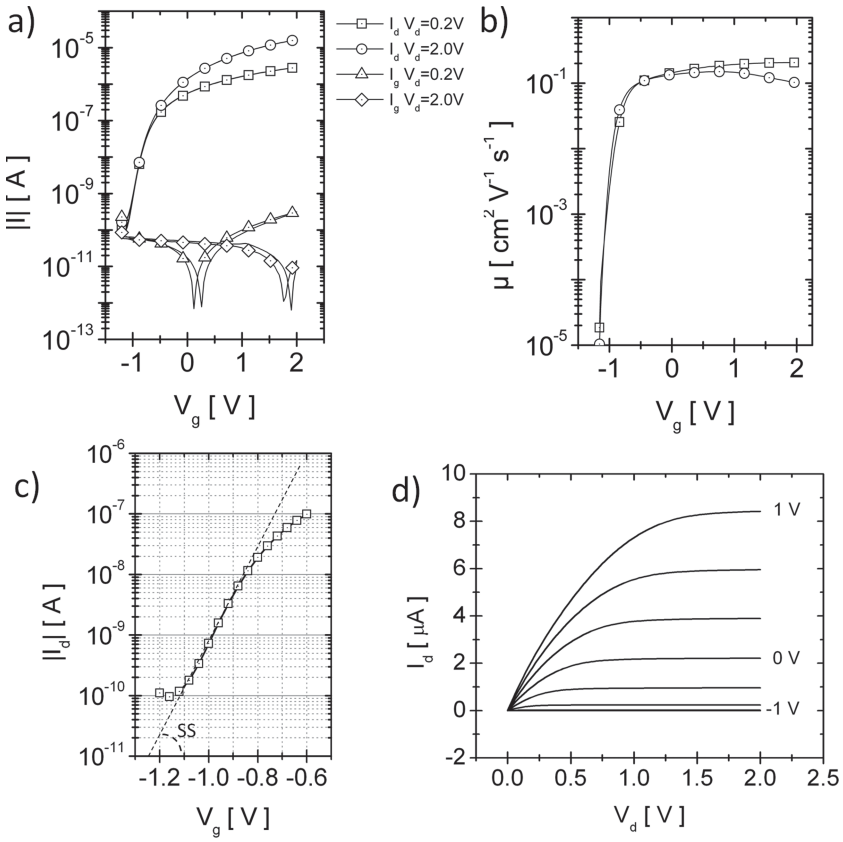

Figure 2. Transfer characteristic curves (a,c), mobility vs. V_g plot (b) and output characteristic curves (d) of optimized low voltage *n*-type P(NDI2OD-T2) OFETs; in (a) squares and circles represent the drain currents at the linear (V_d = 0.2 V) and the high voltage regime (V_d = 2 V) respectively, triangles and diamonds represent gate leakage currents at the linear and the high voltage regime, respectively; in (c) the subthreshold slope is also reported; curves in (d) have been taken at V_g values ranging from –1 V to 1 V with steps of 0.25 V.

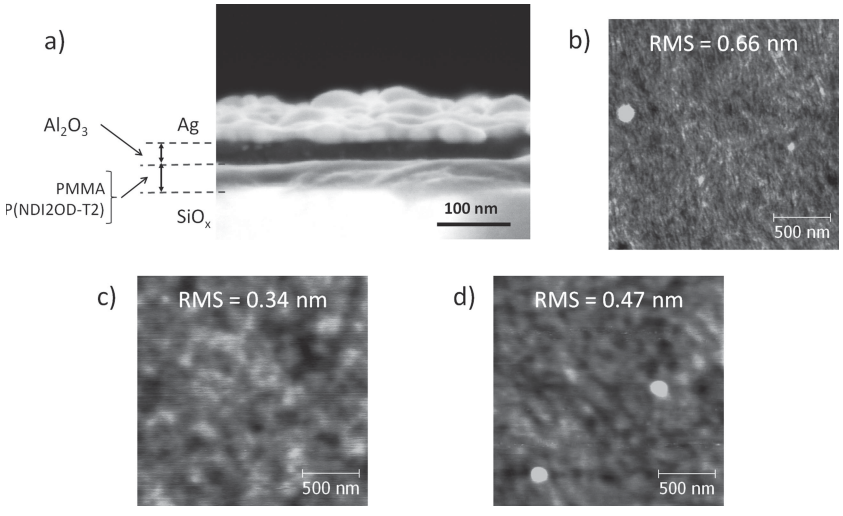

Figure 3. (a) SEM micrograph of a multilayer stack comprising P(NDI2OD-T2) (30 nm thick), PMMA (~10 nm thick) and alumina (~30 nm), obtained from the section of an OFET fabricated on a silicon dioxide substrate. AFM topography (scan size 1 μm × 1 μm) of a P(NDI2OD-T2) film (30 nm thick) (b), a P(NDI2OD-T2) film (30 nm thick) coated with 10 nm of PMMA (c) and a P(NDI2OD-T2) film (30 nm thick) plus a PMMA layer (10 nm thick), all coated with a 30 nm thick alumina layer (d).

that very flat surfaces are obtained at each deposition step. Moreover a planarization effect is induced by the deposition of subsequent layers on P(NDI2OD-T2) surface: a roughness of ~0.7 nm (r.m.s. value) was calculated on the typical fibrils-like topography of bare P(NDI2OD-T2) surface (Figure 3b); this reduces down to ~0.4 nm when ~10 nm of PMMA are deposited on top (Figure 3c). After alumina deposition (30 nm), a very similar topography can be observed except for a slightly increased roughness, reaching ~0.5 nm (Figure 3d).

We have previously evidenced the low *SS* of low voltage P(NDI2OD-T2) OFETs demonstrated in this work (Figure 2c). The subthreshold behavior of an OFET is a direct consequence of the number of interfacial and bulk traps populating the semiconductor layer;[70] accordingly, the systematic investigation of the subthreshold slopes of devices obtained using different processing condition can be informative of any eventual modification and/or contamination of the interface between the semiconductor and the dielectric, eventually inherent to the technology employed (like PLD for alumina).

The maximum density of interfacial trap sites (N_{SS}^{max}) can be obtained using the following equation:[70]

$$N_{SS}^{\max} = \left[SS \times \log(e) / (kT/q) - 1 \right] \times C_{die}/q \quad (4)$$

According to Equation (4), an invariant number of interfacial trap sites entails a linear proportionality between *SS* and $1/C_i$. We have plotted the dependence of *SS* and N_{SS}^{max} on $1/C_i$ on the whole range of capacitances attainable with hybrid dielectrics reported in this work (**Figure 4**). A very clear linear dependence of *SS* vs. $1/C_i$ can be observed for capacitance values in the range between 20 and 130 $nFcm^{-2}$ obtained employing for the alumina and for the PMMA layers a maximum thickness of 300 nm and 100 nm, and a minimum thickness of 30 nm and 10 nm, respectively (Figure 4a); such a scenario corresponds to an almost constant N_{SS}^{max}, in the range of 5×10^{11}–6×10^{11} $cm^{-2}eV^{-1}$ (Figure 4b). On the one hand, these are very low values when compared to the literature,[48] demonstrating a low defectivity of the semiconductor-dielectric interface. On the other, and very importantly, no specific dependence was observed between N_{SS}^{max} and the thickness of PMMA in this capacitance range, i.e. PMMA layers down to 10 nm thick are extremely efficient

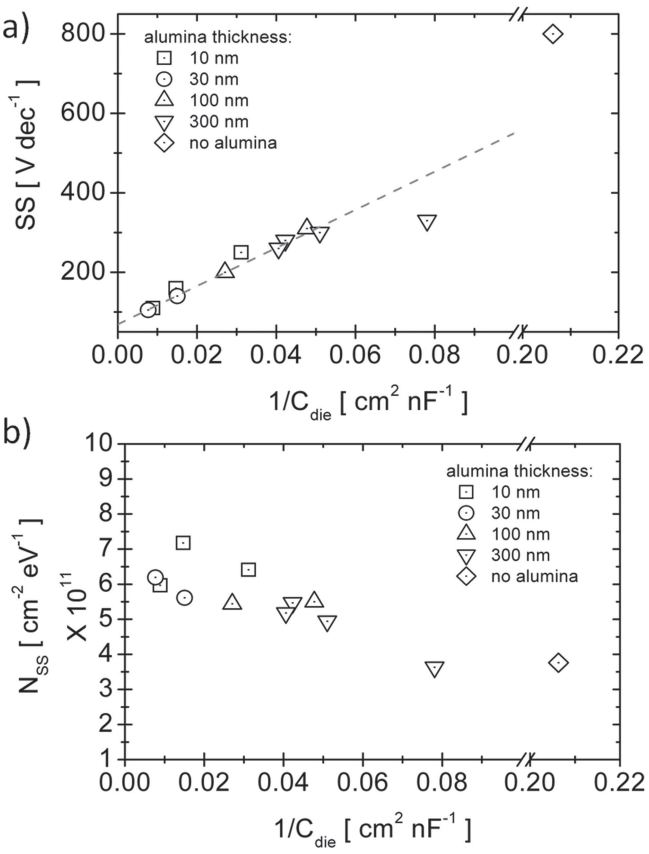

Figure 4. *SS* (a) and N_{SS}^{max} (b) vs. the inverse of dielectric capacitance C_{die}; each color and symbol refers to a specific thickness of the alumina layer; for each value of alumina thickness different capacitances are obtained by adjusting PMMA thickness. In the *SS* plot, the linear fit is also reported (dashed red line).

in protecting the active layer from possible contamination during PLD deposition. Within the same capacitance range, OFETs with just 10 nm thick alumina layer exhibit a small deviation of *SS* from the linear tendency line of Figure 4a (black circles), corresponding to a small increase of the interfacial trap sites (up to 7×10^{11} cm^{-2}eV^{-1}). Such a slight degradation of the subthreshold regime can be likely attributed to a contamination occurring during the gate electrode vapor deposition on top of an incomplete alumina protective layer. SEM images taken on a thin layer of PLD-grown alumina 10 nm thick revealed the presence of several pinholes on its surface (Figure S4), further supporting the previous hypothesis.

A different behavior can be observed for capacitances below 20 nFcm^{-2} ($t_{Al_2O_3} \geq 300$ nm, $t_{PMMA} \geq 40$ nm), where N_{SS}^{max} as low as 4.0×10^{11} cm^{-2}eV^{-1} were measured for OFETs with and without alumina. However, such small differences are apparently correlated to the overall capacitance value and independent on the PMMA and alumina thicknesses: for example bilayers comprising 100 nm thick PMMA show $N_{SS}^{max} = 5.5 \times 10^{11}$ cm^{2}eV^{-1} with a 100 nm thick alumina layer ($C_{die} = 21$ nFcm^{-2}) and $N_{SS}^{max} = 3.6 \times 10^{11}$ cm^{2}eV^{-1} with a 300 nm one ($C_{die} = 13$ nFcm^{-2}). The reason for this behavior is not well understood at the moment and its detailed explanation is beyond the scope of the present work.

So far we have illustrated an effective method for the downscaling of OFETs operation voltages, showing high performance devices working at maximum V_g and V_d of 2 V with high apparent mobility values. It is worth stressing at this point the effect of reduced lateral applied voltage (V_d) on the device performance when reducing the operating voltages (both V_g and V_d). While vertical electric fields can be held high owing to the high dielectric capacitance, lateral electric fields are correspondingly reduced with respect to high voltage devices if the channel length is kept the same, as in the present case (20 μm to 5 μm). Such disproportioning of the electric field components results in a variation of the transistor bias point between the high-voltage and low-voltage devices. This in turn may affect the balance between the contact resistances and the channel resistances, which competitively define the overall electrical properties of an OFET. This is especially true in the case of P(NDI2OD-T2) OFETs, for which the contact resistances are known to depend on the applied V_d, i.e., on the lateral electric field between Source and Drain in TGBC devices.[22] This means that, in order to properly compare low voltage with high voltage devices, the two components of the total resistances of the devices (channel and contact resistances) should be separately accounted for. Therefore, we have extracted the contact resistances R_C and the intrinsic mobility μ_{int} (i.e., the mobility values without the contact resistance contribution) of the low voltage *n*-channel OFET of Figure 2, and of a high voltage P(NDI2OD-T2) OFETs, fabricated with identical Source and Drain electrodes and a 600 nm thick PMMA as the dielectric layer ($C_{die} \sim 5$ nFcm^{-2}). R_C and μ_{int} were obtained using the differential method,[23,71] which is a method that allows to account for the dependence on the lateral field (i.e. on V_d), therefore better suited to describe contact resistances in P(NDI2OD-T2) OFETs.[22] These parameters were extracted and reported in **Table 1**: as expected much higher R_C are extracted in low-voltage OFETs (34 kΩ cm) compared to high-voltage devices (8.8 kΩ cm). Anyhow, comparable intrinsic mobilities were calculated (~0.5 cm^{2}V^{-1}s^{-1} and of ~0.3 cm^{2}V^{-1}s^{-1}, respectively). Following the previously reported dependence of μ on κ by F. Yan and co-workers[25,29] for P(NDI2OD-T2) OFETs, this is an important observation because it indicates that in the devices

Table 1. Summary of the parameters extracted with the differential method from P(NDI2OD-T2) low voltage OFETs. All the curves were fitted in a V_g range within 3 V and 4 V; as a comparison, the results obtained with high voltage standard PMMA devices are also reported. In the table threshold voltage (V_{th}) mean values in the linear regime and standard deviations (St. Dev.) are also reported.

Dielectric layer (thickness)	C_i [nFcm^{-2}]	V_g/V_d [V/V]	μ_{int} [cm^{2}V^{-1}s^{-1}]	R_C [kΩcm]	*Mean* V_{th} [V]	*St. Dev.* V_{th} [V]
Al_2O_3/PS (30 nm/ 10 nm)	78.1	4.2/0.5	0.66	71	–0.15	0.05
Al_2O_3/PMMA (30 nm/40 nm)	77.4	3.0/0.5	0.32	34	–0.8	0.14
PMMA (600 nm)	4.85	50/5	0.5	8.8	–1.75	0.65

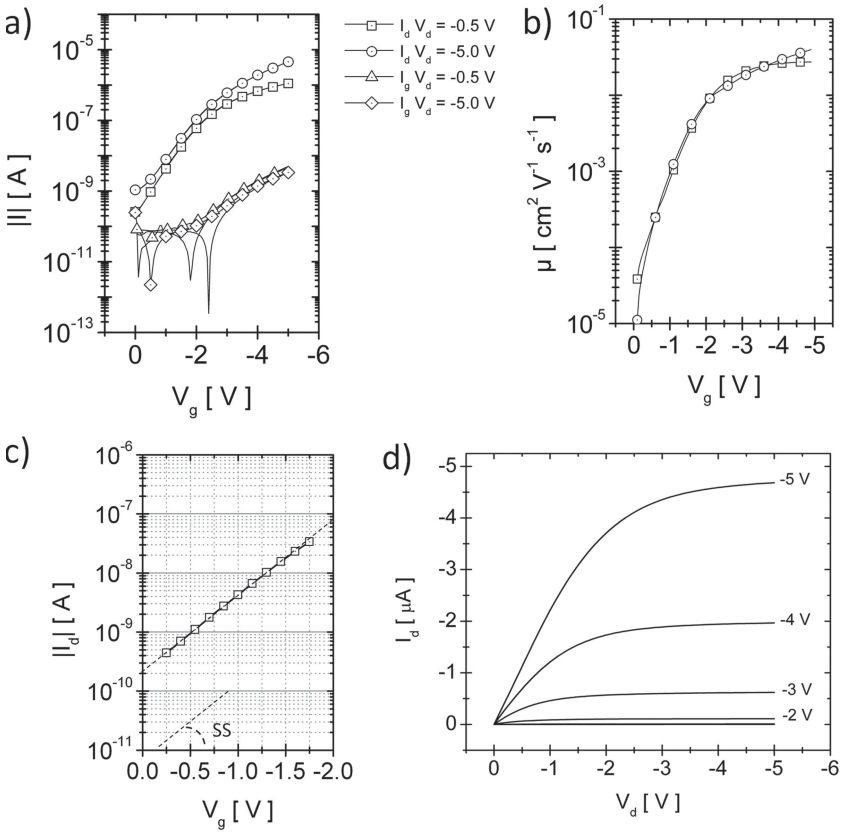

Figure 5. (a) Transfer characteristic curves, (b) mobility vs. V_g plot and (d) output characteristic curves of optimized low voltage *p*-type pBTTT OFETs; in (a) squares and circles represent the drain currents at the linear (V_d = –0.5 V) and the saturation regime (V_d = –5 V) respectively, and triangles and diamonds represent gate leakage currents at the linear and the saturation regime, respectively; in (c) the subthreshold slope is also reported.

gated through the hybrid nanodielectrics, the energetic at the semiconductor–dielectric interface is entirely defined by the ultra-thin low-κ dielectric layer in direct contact with the semiconductor (i.e., PMMA), with no apparent influence of the higher κ alumina layer.

To further confirm this point, we tested the possibility to act on the transport properties of P(NDI2OD-T2) by substituting the PMMA interlayer with a lower κ PS interlayer (κ = 2.6). An even higher intrinsic mobility, up to ~0.7 cm^{2}V^{-1}s^{-1} – was obtained in such case, in agreement with expectations.

We further integrated the hybrid dielectrics with pBTTT semiconductor to demonstrate low-voltage *p*-channel OFETs, the complementary part of *n*-channel devices needed to realize robust logic circuits.[17] In **Figure 5** the electrical characterization of a low voltage pBTTT OFET with a capacitance of ~65 nFcm^{-2} (PMMA thickness: 40 nm; alumina thickness: 30 nm) is reported. At V_g = 5 V we obtained an I_{ON}/I_{OFF} current ratio approaching 10^4 (calculated at V_g = –5 V for I_{ON} and at V_g = 0 V for I_{OFF}, keeping V_d = 5 V), an apparent mobility of 0.04 cm^{2}V^{-1}s^{-1}, a V_{th} of –2.2 V and a maximum leakage density of 10^{-7}A cm^{-2}. Gate voltages of –10 V are needed to obtain a state-of-the-art apparent mobility of 0.1 cm^{2}V^{-1}s^{-1}. Output curves, reported in Figure 5d highlight optimal injection and good *p*-channel modulation. It can be observed that much higher gate voltages are necessary to turn completely ON pBTTT devices with respect to P(NDI2OD-T2), leading to slightly higher leakage levels of operative OFETs (which are instead comparable at V_g = 2 V). In Figure 5c we highlight the subthreshold slope of such devices, which was calculated to be ~750 mVdec^{-1}. High *SS* values are intrinsic to pBTTT semiconductor[32] and not a direct consequence of the coupling with high capacitance dielectrics.

The low voltage *n*-channel and *p*-channel OFETs were combined to form low voltage complementary inverters (**Figure 6**a). Voltage transfer characteristics of the inverters (Figure 6b) display a clear inversion and a gain close to 10 already at V_{DD} = 2 V, with a Noise Margin (NM) of 0.35 V (17.5% of V_{DD}). The inverters appear unbalanced at very low voltage due to the difference in *SS* between *n*-channel (Figure 2c) and *p*-channel (Figure 5c) devices, while they are almost totally balanced at 5 V, attaining high gain (>15), high NM (28.0% of V_{DD}) and an inversion threshold V_{inv} approaching V_{DD}/2. Such outstanding results demonstrate the suitability of the developed high capacitance, nanoscale hybrid dielectrics for low-power and robust, organic complementary logic circuits.

3. Conclusion

We developed a simple and high yield method for the realization of low voltage TG OFETs operating already at 1 V using high capacitance, hybrid nanoscale dielectrics based on common materials like PMMA and alumina. The key factor of such approach is represented by a double layer structure for the dielectric, composed by an ultra-thin, low-κ organic buffer layer in direct contact with the active semiconducting phase, and an ultra-thin high-κ alumina on the top, able to improve the electrical strength of the dielectric and to reduce leakage currents through it. The high yield of the process was made possible by the use of PLD for the room-temperature fabrication of the alumina layer.

By adopting these dielectrics, we have demonstrated high performance *n*-channel and *p*-channel TG OFETs with capacitances up to 0.25 μFcm^{-2} and very low gate leakage density even in unpatterned devices. Through a deep investigation of P(NDI2OD-T2) OFETs characteristics we clarified that, in such a hybrid device structure, the energetics at the semiconductor-dielectric interface are solely defined by the ultrathin (10 nm) organic dielectric interlayer in direct contact with the semiconductor: by using a polystyrene interlayer, intrinsic mobility up to 0.7 cm^{2}V^{-1}s^{-1} could be obtained. This remarkable result indicates that ultra-thin dielectric polymer layers can be effectively adopted at the interface with polymer semiconductors to decouple the channel from the effect of high-κ oxides physically deposited on top, opening vast opportunities for the further

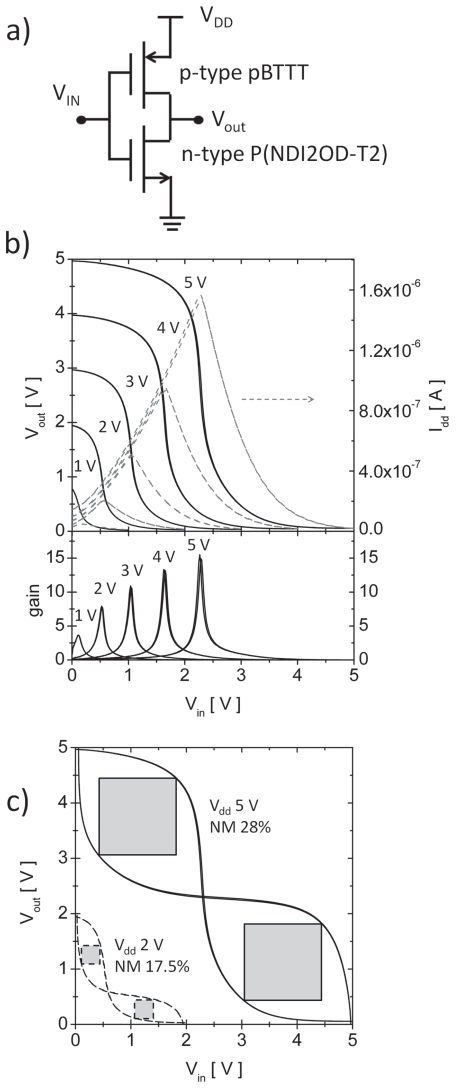

Figure 6. a) Circuit schematic of a complementary inverter realized in this work with P(NDI2OD-T2) (n-type) and pBTTT (p-type) semiconductors. b) Voltage transfer characteristics, static currents (I_{DD}) and gains as a function of input voltages from V_{DD} = 1 V to V_{DD} = 5 V. c) Noise margin extracted at V_{DD} = 2 V and V_{DD} = 5 V.

development of low-leakage, high performance hybrid dielectrics compatible with organic electronics. By showing also the possibility to adopt this approach to develop complementary organic inverters displaying clear inversion and a gain close to 10 already at V_{DD} = 2 V, we have therefore demonstrated that the proposed hybrid approach for the realization of ultra-low voltage OFETs can be a candidate for the cost-effective, room-temperature manufacturing of organic circuits with high yield.

4. Experimental Section

Thoroughly cleaned 1737F glass or SiO_2 were used as substrates. Au contacts were defined by a lift-off photolithographic process with a 0.7 nm thick Cr adhesion layer. The thickness of the Au contacts was 30 nm. Patterned substrates were cleaned in a sonic bath in isopropyl alcohol for 2–3 min before deposition of the semiconductor or the dielectric.

Double layer capacitors (sketched in Figure 1a) were fabricated as follow: PMMA (Sigma-Aldrich) with M_w = 120 kg mol^{-1} was spun from n-butylacetate (varying from 40 gL^{-1} to 5 gL^{-1}, filtered with a 0.45 µm PTFE filter) in air at 6000 rpm for 60 s. In this way PMMA thicknesses within 100 nm and 10 nm were obtained. After the PMMA deposition, the devices were annealed under nitrogen, on a hot-plate, at 80 °C for 4 h. On the top of the PMMA layers Al_2O_3 was grown using PLD. The mechanical properties and structural features of Al_2O_3 can be tailored by tuning the process conditions; the product can range from hard, fully-dense and compact layers[58,72] to columnar and porous microstructures.[72] The Al_2O_3 coating was deposited at room temperature by PLD in a stainless steel vacuum chamber. An excimer laser (COMPEX Coherent – wavelength: 248 nm) was used to ablate a pure (99.99%) polycrystalline Al_2O_3 target with an incidence angle of 40° and a repetition rate of 20 Hz. Incidentally, pulse frequencies up to 600 Hz could be applied with industrially available lasers, drastically increasing the deposition rate. The fluence was adjusted to 2.38 J/cm^2 so as to minimize droplet ejection. A deposition rate of 0.78 nm s^{-1} has been employed. The depositions were carried out at different pressures (0.1, 1, 2, 3, 4, and 5 Pa) and background gases (O_2, N_2 and Ar), the best performance of the devices being attained with Ar at 2 Pa.

Single layer capacitors were also fabricated—without PMMA—growing Al_2O_3 directly onto the gold patterned glass substrate, using the same technique described above.

The *n*-type OFETs (sketched in Figure 1c) were fabricated as follows: P(NDI2OD-T2) was purchased by from Polyera Corporation (Activink N2200). After filtering through a 0.2 µm polytetrafluoroethylene (PTFE) filter, a solution of P(NDI2OD-T2) (9 g L^{-1} in 1,2-dichlorobenzene and 5 g L^{-1} in toluene) was deposited by spin-coating at 1000 rpm for 90 s in a nitrogen glove box on gold-patterned substrates described above. The semiconductor was then annealed for 14 h at 120 °C on a hot plate in a nitrogen atmosphere. PMMA (Sigma-Aldrich) with M_w = 120 kg mol^{-1} was spun from n-butylacetate or 2-butanone (varying from 40 g L^{-1} to 5 g L^{-1}, filtered with a 0.45 µm PTFE filter) in air at 6000 rpm for 60 s. The dielectric-layer thicknesses within 100 nm and 10 nm were obtained. After the dielectric deposition, the devices were annealed under nitrogen, on a hot-plate, at 80 °C for 4 h. Al_2O_3 layers were realized using the same procedures adopted for capacitors. 30 nm thick gate Al electrodes were thermally evaporated as gate contacts.

The *p*-type OTFTs (sketched in Figure 1c) were fabricated as follows: gold contacts of source and drain were cleaned with 3 min of O_2 plasma. A standard thiol-based SAM 2H-perfluorodecanethiol (PFDT) treatment was subsequently applied to the Au-surface of the contacts. The PFDT was performed to increase the Au work function (4.7–5.2 eV), thus facilitating the hole injection to the HOMO level of pBTTT.[73] Samples were immersed for 20 min into a PFDT solution of isopropanol, and rinsed with isopropanol. The pBTTT was purchased from Ossila. The pBTTT was diluted in a solution of anhydrous dichlorobenzene at a concentration of 5 mg mL^{-1} being placed on a 100 °C hotplate for complete dilution. The solution was filtered with a 0.2 µm polytetrafluoroethylene (PTFE) syringe filter and spin-coated at 2000 rpm for 90 s in a nitrogen glovebox. The films of pBTTT were annealed in three phases: first at 80 °C for 10 min to remove the solvent, then up to 180 °C for 10 min and finally cooled down slowly through the mesophase region. Dielectric layers and gate contacts were realized using identical procedure of *n*-type OFETs described above.

The electrical characteristics of capacitors and transistors were measured in a nitrogen glovebox on a Wentworth Laboratories probe station with an Agilent B1500A semiconductor device analyzer and Agilent Precision LCR Meter. The transistor parameters, such as charge carrier mobility, were calculated using the gradual channel approximation for field-effect transistors in the linear and saturation regimes respectively (see SI). The surface morphology of the films was obtained with an Agilent 5500 Atomic Force Microscope operated in the Acoustic Mode. The thicknesses of the polymer films were measured with a KLA Tencor Alpha-Step Surface Profiler.

The cross-sections of the samples were examined by field emission scanning electron microscopy (SEM) using a Zeiss Supra 40 microscope. The electron accelerating voltage was set at 2 kV for imaging, with and aperture diameter of 20 µm.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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